Amendments In The Claims

Claims 1 - 7 (canceled);

WHAT FOLLOWS NOW ARE NEWLY PRESENTED CLAIMS

Claim 8 (previously added as claim 7 in the parent case, there a re-presented version of claim 1 for (de-serialization) and re-resented here with a spelling correction);

8. A de-serializing circuit for a receive sub-vector that is a subset of Q-many bits associated with a previous serialization and whose de-serialized version is one member of a sequential plurality of similarly de-serialized received sub-vectors that combine to form a complete receive vector that is subsequently operated upon by a test system, the de-serializing circuit comprising:

Q-many MUX's, each MUX having at least (Q+1)-many data inputs to which are coupled the bits of a receive sub-vector to be de-serialized, the correspondence between the (Q+1)-many data inputs and the bits of the receive sub-vector to be de-serialized being the same for each MUX;

each MUX having an output bit that will represent the signal at one of the (Q+1)-many data inputs of that MUX;

Q-many latches, each latch associated with a MUX and having an input coupled to the output bit of its associated MUX and also having an output coupled to an input of its associated MUX;

each MUX also having a collection of at least m control inputs, $2^m \geq Q+1$, to which are coupled, for each MUX, a corresponding separate collection of control signals whose values indicate which of the (Q+1)-many data inputs will have its signal coupled to the output bit of that MUX;

a memory having an address and containing addressable locations each storing a set of control signal values of ($Q \cdot m$)-many bits representing the respective values of the m-many control signals for the Q-many MUX's and also having data outputs coupling members of the set of control signal values to the control inputs of their respective MUX's;

the output bits for the Q-many MUX's forming an accumulated latched collection of sub-vectors constituting a de-serialized receive vector, according to a de-serialization defined by the addressed set of control signal values; and

a programmatically controlled address applied to the memory and that selects a pre-defined de-serialization stored in the memory and that is to be performed upon the receive sub-vectors.

Claim 9 (new, re-presented combination of claims 4 and 5 (for combined mapping and serialization));

9. A combined mapping and serialization circuit for altering an original transmit vector of Q-many bits whose altered version is to be applied to a DUT, the combined mapping and serialization circuit comprising:

n-many MUX's, $n \leq Q$, each MUX having at least Q-many data inputs to which are coupled the Q-many bits of an original transmit vector to be altered, the correspondence between the Q-many data inputs and the Q-many bits of the original transmit vector to be altered being the same for each MUX;

each MUX having an output bit that will represent the signal at one of the Q-many data inputs of that MUX;

each MUX also having a collection of at least m control inputs, $2^m \geq Q$, to which are coupled, for each MUX, a corresponding separate collection of control signals whose values indicate which of the Q-many data inputs will have its signal coupled to the output bit of that MUX;

a memory having an address and containing addressable locations each storing a set of control signal values of $(m \cdot n)$-many bits representing the respective values of the m-many control signals for the n-many MUX's and also having data outputs coupling members of the set of control signal values to the control inputs of their respective MUX's;

the output bits for the n-many MUX's forming an alteration of the original transmit vector, the alteration constituting one of: (a) a mapped transmit vector whose Q-many bits are re-ordered according to a mapping defined by the addressed set of control signal values; or (b) a sequential collection of non-re-ordered signals, each collection being one of a plurality of transmit sub-vectors each having less than Q-many bits and the sequence of the collections being according to a serialization defined by the addressed set of control signal values; or (c) a sequential collection of re-ordered signals, each collection being one of a plurality of transmit sub-vectors each having less than Q-many bits that have also been re-ordered according to a mapping defined by the addresses set of control signal values, and the sequence of the collections being according to a serialization defined by the addressed set of control signal values; and

a programmatically controlled address applied to the memory and that selects a pre-defined alteration stored in the memory and that is to be performed upon the original transmit vector.

Claim 10 (new, re-presented combination of claims 6 and 7 for (for combined reverse mapping and de-serialization));

10. A de-serialization and reverse mapping circuit for a series of receive sub-vectors each of which is a subset of Q-many bits associated with a previous serialization and whose de-serialized version and reverse mapped version is a complete receive vector that is subsequently operated upon by a test system, the de-serializing and reverse mapping circuit comprising:

Q-many MUX's, each MUX having at least (Q+1)-many data inputs to which are coupled the bits of a receive sub-vector to be de-serialized, the correspondence between the (Q+1)-many data inputs and the bits of the receive sub-vector to be de-serialized being the same for each MUX;

each MUX having an output bit that will represent the signal at one of the (Q+1)-many data inputs of that MUX;

Q-many latches, each latch associated with a MUX and having an input coupled to the output bit of its associated MUX and also having an output coupled to an input of its associated MUX;

each MUX also having a collection of at least m control inputs, $2^m \geq Q+1$, to which are coupled, for each MUX, a corresponding separate collection of control signals whose values indicate which of the (Q+1)-many data inputs will have its signal coupled to the output bit of that MUX;

a memory having an address and containing addressable locations each storing a set of control signal values of (Q·m)-many bits representing the respective values of the m-many control signals for the Q-many MUX's and also having data outputs coupling members of the set of control signal values to the control inputs of their respective MUX's;

the output bits for the Q-many MUX's forming an accumulated latched collection of sub-vectors constituting a de-serialized and reverse mapped receive vector, according to a de-serialization and a reverse mapping defined by the addressed set of control signal values; and

a programmatically controlled address applied to the memory and that selects a per-defined de-serialization/reverse mapping combination stored in the memory and that is to be performed upon the sequence of receive sub-vectors after they have been received and latched.